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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/082,581	05/21/1998	KENJI NAGASE	980673	2888

38834 7590 01/15/2004

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EXAMINER	
WHIPKEY, JASON T	

ART UNIT	PAPER NUMBER
2612	23

DATE MAILED: 01/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/082,581	Applicant(s) NAGASE, KENJI	
	Examiner Jason T. Whipkey	Art Unit 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,7 and 8* is/are allowed.

6)☒ Claim(s) *1-3 and 6* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 C.F.R. § 1.114

1. A request for continued examination under 37 C.F.R. § 1.114, including the fee set forth in 37 C.F.R. § 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 C.F.R. § 1.114, and the fee set forth in 37 C.F.R. § 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 C.F.R. § 1.114. Applicant's submission filed on October 17, 2003, has been entered.

Drawings

2. Corrected drawings were received on October 17, 2003. These drawings are approved.

Response to Arguments

3. Applicant's arguments filed on October 17, 2003, with regard to claim 1 have been fully considered but they are not persuasive.

Applicant amended claim 1 to recite the limitation, "wherein the power-off signal stops operation of the first circuit and the second circuit and discharges residual

charges of the capacitor by said short circuit". However, this amendment still does not make claim 1 patentable over the prior art cited in the final rejection.

It is inherent that when the circuit shown in Deaver's figure loses power, the operation of the first and second circuits will cease. Therefore, the loss of power will also cause capacitor 24 to discharge, as described in the rejection.

4. Applicant's arguments, see the bottom of page 7 through the top of page 8, filed October 17, 2003, with respect to claim 4 have been fully considered and are persuasive. The rejection of claim 4 has been withdrawn.

Claim 4 is now objected to because it is dependent on rejected claim 1.

5. Applicant's arguments, see page 6, filed October 17, 2003, with respect to claim 5 have been fully considered and are persuasive. The rejection of claim 5 has been withdrawn.

6. Applicant's arguments filed October 17, 2003, with regard to claim 6 have been fully considered but they are not persuasive.

Iwamoto, Sawanobori, and Takeda contain subject matter that is within the realm of power supplies. The presence in the disclosures of apparatuses that are to receive power generated by the disclosed power supplies does not negate the usefulness of the three references. As stated in the final rejection, it would have been obvious to one of ordinary skill in the art to combine the references' teachings about power supplies.

7. Applicant's arguments, see page 9, filed October 17, 2003, with respect to claims 7 and 8 have been fully considered and are persuasive. The rejection of claims 7 and 8 has been withdrawn.

Claim Rejections - 35 USC § 103

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claims 1-3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Josephson in view of Deaver.

Regarding claim 1, Josephson discloses a power supply circuit, shown in Figure 1, with a first circuit for producing a positive polarity voltage at +12 V and +5 V output terminals, shown on the right side of the figure. This first circuit consists of rectifier 48, which includes capacitors 62 and 66 (column 4, lines 41-50), and a chopper circuit, which consists of electrical switch means 44 and transistor switch 24. Switch 24 turns on and off repeatedly to create a "chopped" output from transformer 22 (column 3, lines 44-52, and column 4, lines 13-27).

A second circuit, consisting of rectifier 16, diode 110, and capacitors 114 and 118, produces a negative polarity voltage of -12 V at an output terminal, shown on the right side of Figure 1. Ground terminal GND, also shown on the right side of Figure 1, provides a reference for the positive and negative terminals.

Josephson is silent with regard to including means for short-circuiting the positive and negative terminals upon loss of source power.

Deaver discloses a discharge circuit for capacitors in a power supply. The power supply shown in the figure includes a first circuit that generates a positive polarity voltage, consisting of the two diodes shown on the right of full-wave rectifier 12 and connected to the positive node. This node is connected to a capacitor 14. The positive polarity voltage is output via terminal +VOUT.

The power supply also includes a second circuit that generates a negative polarity voltage, consisting of the two diodes shown on the left of full-wave rectifier 12 and connected to the negative node. This node is connected to a capacitor 16. The positive polarity voltage is output via terminal +VOUT. The transformer 10 is center-tapped to ground. When the AC voltage is removed capacitor 24 charges, which allows current to flow through the emitter-collector junction of PNP bipolar junction transistor 28 (column 3, lines 62-65). This discharges capacitors 14 and 16 (column 3, lines 66-67).

As stated in column 1, lines 61-66, this serves the purpose of preventing the discharge of hazardous amounts of charge stored in the capacitors, which makes the power supply safer. For this reason, it would have been obvious at the time of invention to have Josephson include a discharge means between the positive terminals and the negative terminals.

Regarding claims 2 and 3, transistor 28 in Deaver is a switching element, and resistor 30 is a current-limiting element. Both are located between the positive and negative terminals.

10. Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwamoto in view of Sawanobori and further in view of Takeda (U.S. Patent No. 5,475,500).

Iwamoto discloses a power supply circuit with a circuit generating a positive polarity voltage (3 and the node connecting to terminal V_{DD}; see column 2, lines 58-64), a terminal for outputting the positive voltage (V_{DD}), a circuit generating a negative polarity voltage (3, the node connecting to terminal V_{SS1}; see column 2, lines 58-64), and a terminal for outputting the negative voltage (V_{SS2}, when SW3 and SW4 are closed).

Iwamoto shows that capacitor C_2 (and therefore terminals V_{DD} and V_{SS2}, with voltages of +5V and -5V, respectively), shown in Figure 1, may be short-circuited via switch SW_5 upon power off (column 5, lines 43-51). This eliminates a residual voltage between the terminals (column 5, lines 51-53). Consequently, the significant teaching provided by Iwamoto is that short-circuiting two output terminals of a power supply eliminates a residual voltage between the terminals.

Iwamoto is silent with regard to using the power supply circuit with a CCD imager.

Sawanobori shows that CCD 15 uses a power supply 15 consisting of a 15V line and a -9V line (Drawing 1). When power is lost on -9V line S3, discharge circuit 18 discharges the line to prevent "deterioration or destruction of the image pickup element due to application of a negative voltage" (constitution, lines 15-21). Therefore, the significant teachings provided by Sawanobori are: (a) that CCDs may require power

supplies outputting separate positive and negative voltages, and (b) that a discharge circuit may prevent deterioration of or destruction to a CCD.

A power supply, such as the one described by Iwamoto, may operate irrespective of the device to which it is attached. Additionally, CCDs may operate irrespective of the structure of the power supply to which it is connected, assuming it receives the correct voltage or voltages. Since CCDs need a power supply in order to function, which was the conclusion reached by teaching (a) of Sawanobori, it would have been obvious to one of ordinary skill in the art at the time of invention to connect a CCD to a power supply. Acknowledging the teaching of Iwamoto and teaching (b) of Sawanobori as described above, it would have been obvious to one of ordinary skill in the art at the time of invention to discharge two terminals because the discharge eliminates a residual voltage between two terminals, and a discharge circuit may prevent deterioration of or destruction to a CCD.

Iwamoto is silent with regard to including a microcomputer and using it to produce the power-off signal.

Takeda discloses an imaging device controlled by microcomputer 16. As shown in the flowchart of Figure 7B, when microcomputer 16 detects a power off command (column 7, lines 58-65), it initiates a shutdown procedure for power supply parts 2a, 4, and 5 (column 8, lines 28-41). An advantage to using a microcomputer to produce a power-off signal is that the circuitry used to control the signal may be reused during other operations, thus simplifying the hardware design. For this reason, it would have

been obvious at the time of invention to have Iwamoto perform shutdown control using a microcomputer.

Allowable Subject Matter

11. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

No prior art could be located that teaches or fairly suggests the power supply circuit described, particularly one with a first output terminal connected to a chopper circuit and a second output terminal connected to a fly-back circuit, wherein the second terminal has no connection to the chopper circuit.

12. Claims 5, 7, and 8 are allowed.

Regarding each of these claims, no prior art could be located that teaches or fairly suggests the power supply circuit described, particularly one with a first output terminal connected to a chopper circuit and a second output terminal connected to a fly-back circuit, wherein the second terminal has no connection to the chopper circuit.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason T. Whipkey, whose telephone number is (703) 305-1819. The examiner can normally be reached Monday through Friday from 8:30 A.M. to 6:00 P.M. eastern standard time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber, can be reached on (703) 305-4929. The fax phone number for the organization where this application is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 306-0377.

JTW

JTW
January 11, 2004

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600